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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/829,146	04/09/2001	Thomas N. Toombs	M-10234-1D US	1045

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PARSONS HSUE & DE RUNTZ LLP
655 MONTGOMERY STREET
SUITE 1800
SAN FRANCISCO, CA 94111

EXAMINER

KIM, HONG CHONG

ART UNIT	PAPER NUMBER
2186	41

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/829,146

Applicant(s)

TOOMBS ET AL.

Examiner

Hong C Kim

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 June 2004.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 17-22 and 24-27 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 17-22 and 24-27 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

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Detailed Action

1. Claims 17-22 and 24 -27 are presented for examination. This office action is in response to the amendment filed on 6/1/2004.
2. Again, applicants are requested to supply previous versions (i.e. Version 1.0, 1.1, 1.2, and 1.3) of The MultiMediaCard System Specification because information are not readily available to the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fandrich et al. (Fandrich) U.S. Patent 5,418,752 in view of Kishi et al. (Kishi) U.S. Patent No. 4,841,432 or Noel et al. (Noel) U.S. Pub. No. 2002/00168891.

As to claim 24, Fandrich discloses a memory system (Fig. 2) comprises a plurality of memory groups (col. 3 lines 55-60), each of the memory groups comprising a plurality of memory cells (col. 3 lines 55-60); a plurality of group tags (col. 11 lines 29-38, lock bits, and Fig. 3 Ref. 260), each of the group tags corresponding to one of the memory groups, each of the group tags indicating whether the memory cells under the corresponding memory group are write protected (col. 11 lines 29-38 and Fig. 3 Ref. 260); and wherein any combination

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of the memory groups can be write protected (col. 11 lines 29-38, "corresponding blocks" read on this limitation and Fig. 3 Ref. 260), however, Fandrich does not specifically disclose the number of memory cells in each memory group is configurable. Kishi discloses the number of memory cells in each memory group is configurable (abstract) for the purpose of optimizing flash devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the number of memory cells in each memory group is configurable as shown in Kishi into the invention of Fandrich because it would accommodate optimize flash devices.

Alternatively, Noel discloses the number of memory cells in each memory group is configurable (block 265) for the purpose of optimizing flash devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the number of memory cells in each memory group is configurable as shown in Noel into the invention of Fandrich because it would accommodate optimize flash devices.

As to claim 25, Kishi further discloses the corresponding cells in each memory groups is calculated in real time (col. 5 lines 32-42). Alternatively, Noel further discloses the corresponding cell in each memory groups is calculated in real time (block 265).

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As to claims 26 and 27, Fandrich further discloses a flash memory (Fig. 2 Ref. 20).

4. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harari et al. (Harari) U.S. Patent 5,418,752 in view of Kaki et al. (Kaki) U. S. Patent 5,809,515.

As to claim 17, Harari discloses a memory system (Fig. 1B) comprises a plurality of memory groups, each of the memory groups comprising a plurality of memory sectors, each of the memory sectors (col. 1 line 61 thru col. 2 line 1) comprising a plurality if memory cells; a plurality of sector tags, each of the sector tags corresponds to a memory sector, each of the sector tags (col. 6 lines 41-46) indicating whether the memory cells under the corresponding memory sector are erasable, wherein al the memory cells belong to one memory sector are erasable when the corresponding sector tag is set, wherein any combination of memory sectors in a memory group can be simultaneously erased (col. 1 line 61 thru col. 2 line 1), however, Harari does not specifically disclose a plurality of group tags, each of the group tags corresponds to one of the memory groups, each of the group tags indicating whether the memory cells under the corresponding memory group are erasable, wherein al the memory cells belong to one memory group are erasable when the corresponding group is set, wherein any combination of memory groups can be simultaneously erased.

Kaki discloses a plurality of group tags, each of the group tags corresponds to one of the memory groups, each of the group tags indicating

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whether the memory cells under the corresponding memory group are erasable, wherein all the memory cells belong to one memory group are erasable when the corresponding group is set, wherein any combination of memory groups can be simultaneously erased (col. 7 line 64 thru col. 8 line 14) for the purpose of increasing the memory erasing speed thereby increasing the access bandwidth.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate plurality of group tags, each of the group tags corresponds to one of the memory groups, each of the group tags indicating whether the memory cells under the corresponding memory group are erasable, wherein all the memory cells belong to one memory group are erasable when the corresponding group is set, wherein any combination of memory groups can be simultaneously erased as shown in Kaki into the invention of Harari because it would increase the memory access speed.

5. Claims 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harari et al. (Harari) U.S. Patent 5,418,752 in view of Kaki et al. (Kaki) U. S. Patent 5,809,515 and further in view of Kishi et al. (Kishi) U.S. Patent No. 4,841,432 or Noel et al. (Noel) U.S. Pub. No. 2002/00168891.

As to claim 18, Harari and Kaki disclose the invention as claimed above, however, neither Harari nor Kaki specifically discloses the number of memory sectors in each memory group is configurable. Kishi discloses the number of memory sectors in each memory group is configurable (abstract) for the purpose of optimizing flash devices.

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Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the number of memory cells in each memory group is configurable as shown in Kishi into the combined invention of Harari and Kaki because it would accommodate optimize flash devices.

Alternatively, Noel discloses the number of memory sectors in each memory group is configurable (block 265) for the purpose of optimizing flash devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the number of memory sectors in each memory group is configurable as shown in Noel into the combined invention of Harari and Kaki because it would accommodate optimize flash devices.

As to claim 19, Kishi further discloses the corresponding sectors in each memory group is calculated in real time (col. 5 lines 32-42). Alternatively, Noel further discloses the corresponding sectors in each memory groups is calculated in real time (block 265).

As to claim 20, Harari and Kaki disclose the invention as claimed above, however, neither Harari nor Kaki specifically discloses the number of memory cells in each memory sector is configurable. Kishi discloses the number of

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memory cells in each memory sector is configurable (abstract) for the purpose of optimizing flash devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the number of memory cells in each memory sector is configurable as shown in Kishi into the combined invention of Harari and Kaki because it would accommodate optimize flash devices.

Alternatively, Noel discloses the number of memory cells in each memory sector is configurable (block 265) for the purpose of optimizing flash devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the number of memory cells in each memory sector is configurable as shown in Noel into the combined invention of Harari and Kaki because it would accommodate optimize flash devices.

As to claim 21, Kishi further discloses the corresponding cells in each memory sector is calculated in real time (col. 5 lines 32-42). Alternatively, Noel further discloses the corresponding cells in each memory sector is calculated in real time (block 265).

As to claim 22, Harari further discloses a flash memory (abstract line 1)

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Response to Amendment

6. Applicant's arguments filed on 6/1/04 have been fully considered but they are not deemed to be persuasive.

Applicant's remarks that the references not teaching group tags and sector tags is not considered persuasive.

Kaki discloses group tags (col. 8 lines 2-5) and sector tags (col. 8 lines 5-8).

Applicant's remarks that the references not simultaneously erased is not considered persuasive.

Kaki discloses simultaneously erasing flash memory sectors (col. 1 line 61 thru col. 2 line 1).

Therefore broadly written claims are disclosed by the references cited.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory

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period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835. The Examiner can normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matt Kim, can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

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Washington, D.C. 20231

or faxed to TC-2100:

Official (703) 872-9306

Hand-delivered responses should be brought to Crystal Park II,
2121 Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).

HK

Primary Patent Examiner

August 19, 2004